Electronic Version
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Claims

[c1] 1.A method of building fault tolerant logic functions in an integrated circuit, comprising the steps of:
creating an integrated circuit design description using a hardware design language at the register-transfer level;
adding a fault tolerant operator to the particular logic functions in said integrated circuit design description; and
building redundant copies for the particular logic functions having a fault tolerant operator.

[c2] 2.A method according to claim 1, wherein said integrated circuit design description in said creating step is for a FPGA.

[c3] 3.A method of creating fault tolerant logic functions during design of an integrated circuit using a HDL at the RTL and a logic synthesis tool, comprising the steps of:
creating an integrated circuit design description using the hardware design language at the RTL;
adding a fault tolerant operator to each logic function in said integrated circuit design description;
processing said integrated circuit design description through the logic synthesis tool after said adding step;

and
including a fault redundant scheme in said integrated circuit design description for each logic function having a fault tolerant operator.

[c4] 4.A method according to claim 3, wherein said fault redundant scheme includes building at least three physical copies of each logic function having a fault tolerant operator.

[c5] 5.A method according to claim 3, wherein said integrated circuit design description in said creating step is for a FPGA.

[c6] 6.A system for creating fault tolerant logic functions during design of an integrated circuit using a HDL at the RTL and a logic synthesis tool, the system comprising:
means for creating an integrated circuit design description using the hardware design language at the RTL;
means for adding a fault tolerant operator to each logic function in said integrated circuit design description;
means for synthesizing said integrated circuit design description after said means for adding step; and
means for building fault redundancy into said integrated circuit design description for each logic function having a fault tolerant operator.

[c7] 7.A system according to claim 6, wherein said means for building fault redundancy includes building at least three physical copies of each logic function having a fault tolerant operator.

[c8] 8.A system according to claim 6, wherein said integrated circuit design description in said creating step is for a FPGA.